

### **AMENDMENTS TO THE CLAIMS**

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

#### **LISTING OF CLAIMS:**

1. (original) A semiconductor integrated circuit device comprising:
  - a memory cell having first and second transfer MISFETs, first and second drive MISFETs and first and second load MISFETs, each disposed at an intersection between a pair of complementary data lines and a word line, the first drive MISFET and first load MISFET being cross-coupled with the second drive MISFET and second load MISFET,
  - wherein the first and second transfer MISFETs and the first and second drive MISFETs are formed over the main surface of a semiconductor substrate,
  - wherein a first insulating film is formed over the semiconductor substrate and a first opening is formed in the first insulating film,
  - wherein a first capacitor element is formed over the sidewall and bottom of the first opening, the first capacitor element having, as a lower electrode, a first conductive film formed along the sidewall and bottom of the first opening, as a capacitor insulator film, a second insulating film formed over the first conductive film, and as an upper electrode, a second conductive film formed over the second insulating film,
  - wherein a supply voltage line electrically connected to the first and second drive MISFETs and a reference voltage line electrically connected to the first and second drive MISFETs are formed over the first capacitor element,
  - wherein the lower electrode forms a first storage node of the memory cell by electrically connecting a drain of the first drive MISFET, a drain of the first load

MISFET, a gate electrode of the second drive MISFET and a gate electrode of the second load MISFET, and a second storage node of the memory cell by electrically connecting a drain of the second drive MISFET, a drain of the second load MISFET, a gate electrode of the first drive MISFET and a gate electrode of the first load MISFET, and

wherein the first capacitor element is electrically connected between the first storage node and second storage node, and the supply voltage line, between the first storage node and second storage node, and the reference voltage line, or between the first storage node and the second storage node.

2. (original) A semiconductor integrated circuit device according to Claim 1, wherein the first opening reaches the gate electrode of the first and second drive MISFETs and the drain of the first and second load MISFETs.

3. (original) A semiconductor integrated circuit device according to Claim 1, wherein the second conductive film extends over the first insulating film and is connected, over the first insulating film, to a conductive layer formed above the second conductive film

4. (original) A semiconductor integrated circuit device according to Claim 1, wherein the first and second load MISFETs are formed above the first and second transfer MISFETs and the first and second drive MISFETs, the first load MISFET has a source, a channel region and a drain formed in a first laminate extending in a direction perpendicular to the main surface of the semiconductor substrate and a gate electrode formed over the sidewall of the first laminate via a gate insulating film,

the second load MISFET has a source, a channel region and a drain formed in a second laminate extending in a direction perpendicular to the main surface of the semiconductor substrate and a gate electrode formed over the sidewall of the second laminate via a gate insulating film, and the first insulating film is formed to cover the first and second load MISFETs.

5. (original) A semiconductor integrated circuit device according to Claim 1, wherein the memory cell is formed in a first region over the main surface of the semiconductor substrate, a power supply circuit is formed in a second region over the main surface of the semiconductor substrate,

wherein in a second opening formed in the first insulating film in the second region, a second capacitor element having the first conductive film formed along the sidewall and bottom of the second opening as a lower electrode, the second insulating film formed over the first conductive film as an insulator and the second conductive film formed over the second insulating film as an upper electrode is formed,

wherein the power supply circuit feeds the memory cell an operating voltage, and

wherein the second capacitor element is electrically connected between the operating voltage and ground potential.

6. (original) A semiconductor integrated circuit device according to Claim 5, wherein the bottom of at least one of the first opening and the second opening reaches a third insulating film formed below the first insulating film, and the first and second conductive films each extends over the first insulating film and is connected,

over the first insulating film, to a conductive layer formed above the first insulating film.

7. (Previously Presented) A semiconductor integrated circuit device comprising:

a memory cell having first and second transfer MISFETs, first and second drive MISFETs, and first and second load MISFETs, each disposed at an intersection between a pair of complementary data lines and a word line, the first drive MISFET and first load MISFET being cross-coupled with the second drive MISFET and second load MISFET; and

a power supply circuit,

wherein the memory cell is formed in a first region over the main surface of the semiconductor substrate and the power supply circuit is formed in a second region over the main surface of the semiconductor substrate,

wherein a first insulating film is formed over the semiconductor substrate,

wherein in an opening formed in the first insulating film in the second region, a second capacitor element having, as a lower electrode, a first conductive film formed along the sidewall and bottom of the second opening, as an insulator, a second insulating film formed over the first conductive film, and as an upper electrode, a second conductive film formed over the second insulating film, and

wherein the power supply circuit feeds the memory cell with an operating voltage and the second capacitor element is electrically connected between the operating voltage and ground voltage.

8. (Previously Presented) A semiconductor integrated circuit device according to claim 7, wherein the bottom of the opening reaches a third insulating film formed below the first insulating film, and the first conductive film and the second conductive film each extends over the first insulating film and is connected, over the first insulating film, to a conductive layer formed above the first insulating film.

9. (Previously Presented) A semiconductor integrated circuit device, comprising a first insulating film formed over a semiconductor substrate, an opening formed in the first insulating film, and a capacitor element having, as a lower electrode, a first conductive film formed along the sidewall and bottom of the opening, as a capacitor insulator film, a second insulating film formed over the first conductive film, and as an upper electrode, a second conductive film formed over the second insulating film formed over the sidewall and the bottom of the opening, said capacitor element constituting an analog circuit.

10. (Previously Presented) A semiconductor integrated circuit device according to Claim 9, wherein the bottom of the opening reaches a third insulating film formed below the first insulating film, and the first conductive film and second conductive film each extends over the first insulating film and is connected, over the first insulating film, to a conductive layer formed above the first insulating film.

**Claims 11-20 (canceled without prejudice or disclaimer).**

21. (Previously Presented) A semiconductor integrated circuit device comprising:

a first insulating film formed over a semiconductor substrate; and  
a plurality of openings formed in the first insulating film,  
wherein a capacitor element is formed over the sidewall and bottom of the plurality of openings and has, as a lower electrode, a first conductive film formed along the sidewall and bottom of the openings, as an insulator, a second insulating film formed over the first conductive film, and as an upper electrode, a second conductive film formed over the second insulating film in the plurality of openings.

22. (original) A semiconductor integrated circuit device according to Claim 21, wherein a plurality of interconnect grooves are formed in the first insulating film and an interconnect is formed in the interconnect grooves.

23. (Previously Presented) A semiconductor integrated circuit device according to claim 1, wherein the first and second load MISFETs are formed over the main surface of the substrate,

wherein the first insulating film is formed over the first and second drive MISFETs, the first and second transfer MISFETs and the first and second load MISFETs,

wherein a second opening is formed in the first insulating film,

wherein a second capacitor element is formed over a side wall and bottom of the second opening such that the second capacitor element has, as a lower electrode, a third conductive film formed along the side wall and bottom of the second opening, as a capacitor insulator film, a third insulating film formed over the

third conductive film, and, as an upper electrode, a fourth conductive film formed over the third insulating film,

wherein the first conductive film extends over the first drive MISFET and the first load MISFET and is electrically connected to the first storage node such that the first conductive film is electrically connected to a drain of the first drive MISFET, a drain of the first load MISFET, a gate electrode of the second drive MISFET and a gate electrode of the second load MISFET,

wherein the third conductive film extends over the second drive MISFET and the second load MISFET and is electrically connected to the second storage node such that the third conductive film is electrically connected to a drain of the second drive MISFET, a drain of the second load MISFET, a gate electrode of the first drive MISFET and a gate electrode of the first load MISFET.

24. (Previously Presented) A semiconductor integrated circuit device according to claim 23, wherein the second conductive film and the fourth conductive film are electrically connected to at least one of the supply voltage line or the reference voltage line.

25. (Previously Presented) A semiconductor integrated circuit device according to claim 23, wherein the second conductive film is electrically connected to the fourth conductive film.

26. (Currently Amended) A semiconductor integrated circuit device comprising:

a memory cell having a first and second drive MISFET and a first and a second load MISFET each having a source region and a drain region formed ~~on~~in a substrate,

wherein gate electrodes of the first and second drive MISFETs and the first and second load MISFETs are formed over a main surface of a the substrate;

a first insulating film formed over the first and second drive MISFETs and the first and second transfer MISFETs,

wherein the first insulating film has a first opening and a second opening;

a first capacitor element formed over a side wall and bottom of the first opening such that the first capacitor element has, as a lower electrode, a first conductive film formed along the side wall and bottom of the first opening, as a capacitor insulator film, a second insulating film formed over the first conductive film, and, as an upper electrode, a second conductive film formed over the second insulating film; and

a second capacitor element formed over a side wall and bottom of the second opening such that the second capacitor element has, as a lower electrode, a third conductive film formed along the side wall and bottom of the second opening, as a capacitor insulator film, a third insulating film formed over the third conductive film, and, as an upper electrode, a fourth conductive film formed over the third insulating film,

wherein the first opening is formed to extend over a drain region of the first drive MISFET and a drain region of the first load MISFET, such that the first conductive film is electrically connected to the drain of the first drive MISFET, the



drain of the first load MISFET, the gate electrode of the second drive MISFET and the gate electrode of the second load MISFET,

wherein the second opening is formed to extend over a drain region of the second drive MISFET and a drain region of the second load MISFET, such that the third conductive film is electrically connected to the drain of the second drive MISFET, the drain of the second load MISFET, the gate electrode of the first drive MISFET and the gate electrode of the first load MISFET.

27. (Previously Presented) A semiconductor integrated circuit device according to claim 26, wherein the second conductive film and the fourth conductive film are electrically connected to at least one of a supply voltage line or a reference voltage line.

28. (Previously Presented) A semiconductor integrated circuit device according to claim 26, wherein the second conductive film is electrically connected to the fourth conductive film.

29. (Currently Amended) A semiconductor integrated circuit device comprising:

a memory cell having a first drive MISFET and a second drive MISFET and a first load MISFET and a second load MISFET each having a source region and a drain region formed ~~on~~in a substrate,

wherein gate electrodes of the first and second drive MISFETs and the first and second load MISFETs are formed over a main surface of a ~~the~~substrate;

a first insulating film formed over the first and second drive MISFETs and the first and second load MISFETs,

wherein the first insulating film has a first opening and a second opening;

a first capacitor element formed over a sidewall and bottom of the first opening such that the first capacitor element has, as a lower electrode, a first conductive film formed along the sidewall and bottom of the first opening, as a capacitor insulator film, a second insulating film formed over the first conductive film, and, as an upper electrode, a second conductive film formed over the second insulating film; and

a second capacitor element formed over a sidewall and bottom of the second opening such that the second capacitor element has, as a lower electrode, a third conductive film formed along the sidewall and bottom of the second opening, as a capacitor insulator film, a third insulating film formed over the third conductive film, and, as an upper electrode, a fourth conductive film formed over the third insulating film,

wherein the first conductive film is electrically connected to the drain of the first drive MISFET, the drain of the first load MISFET, the gate electrode of the second drive MISFET and the gate electrode of the second load MISFET, and

wherein the third conductive film is electrically connected to the drain of the second drive MISFET, the drain of the second load MISFET, the gate electrode of the first drive MISFET and the gate electrode of the first load MISFET.

30. (Previously Presented) A semiconductor integrated circuit device according to claim 29, wherein the second conductive film and the fourth conductive

film are electrically connected to at least one of a supply voltage line or a reference voltage line.

31. (Previously Presented) A semiconductor integrated circuit device according to claim 29, wherein the second conductive film is electrically connected to the fourth conductive film.

32. (New) A semiconductor integrated circuit according to claim 1, wherein:  
the first and second drive MISFET and the first and a second load MISFET each include a source region and a drain region formed in the substrate,  
gate electrodes of the first and second drive MISFETs and the first and second load MISFETs are formed over a main surface of the substrate;  
the first insulating film is formed over the first and second drive MISFETs and the first and second transfer MISFETs, and further includes a second opening;  
a second capacitor element is formed over a side wall and bottom of the second opening such that the second capacitor element has, as a lower electrode, a third conductive film formed along the side wall and bottom of the second opening, as a capacitor insulator film, a third insulating film formed over the third conductive film, and, as an upper electrode, a fourth conductive film formed over the third insulating film;  
the first opening is formed to extend over a drain region of the first drive MISFET and a drain region of the first load MISFET, such that the first conductive film is electrically connected to the drain of the first drive MISFET, the drain of the first load MISFET, the gate electrode of the second drive MISFET and the gate electrode of the second load MISFET; and

the second opening is formed to extend over a drain region of the second drive MISFET and a drain region of the second load MISFET, such that the third conductive film is electrically connected to the drain of the second drive MISFET, the drain of the second load MISFET, the gate electrode of the first drive MISFET and the gate electrode of the first load MISFET.

33. (New) A semiconductor integrated circuit according to claim 1, wherein:

the first drive MISFET and second drive MISFET and the first load MISFET and second load MISFET each include a source region and a drain region formed on the substrate,

gate electrodes of the first and second drive MISFETs and the first and second load MISFETs are formed over a main surface of the substrate;

the first insulating film is formed over the first and second drive MISFETs and the first and second load MISFETs, and further includes a second opening;

a second capacitor element formed over a sidewall and bottom of the second opening such that the second capacitor element has, as a lower electrode, a third conductive film formed along the sidewall and bottom of the second opening, as a capacitor insulator film, a third insulating film formed over the third conductive film, and, as an upper electrode, a fourth conductive film formed over the third insulating film;

the first conductive film is electrically connected to the drain of the first drive MISFET, the drain of the first load MISFET, the gate electrode of the second drive MISFET and the gate electrode of the second load MISFET; and

the third conductive film is electrically connected to the drain of the second drive MISFET, the drain of the second load MISFET, the gate electrode of the first drive MISFET and the gate electrode of the first load MISFET.